R-C-NR Structure Based on MOSFET

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Abstract. Paper presents one of the possible realizations of the R-C-NR-network with distributed parameters which is based on metal-oxide-semiconductor field-effect transistor (MOSFET). Device structure is proposed, device operation and layers description are presented. The model of the new device is developed.

Keywords: RC-network, R-C-NR, distributed parameters, MOSFET, admittance matrix

INTRODUCTION

RC-networks with distributed parameters are intended for different analog signal processing operations, particularly can be used for fractional-order devices realization. Fractional-order devices, whose impedance have non-integer frequency dependency, are currently researched and developed for more advanced modelling of the complex dynamic processes.

Lately the RC-networks are successfully fabricated using *thick film technology*, where single layers are created in the form of films deposited onto the dielectric substrate. This technology allows fabricating circuits with different parameters, which, however, cannot be changed after the fabrication during using by electrical way. And it limits the functionality of the circuits. General disadvantages of the film technology, such as inability to implement qualitative active components and low integration scale, also restrict their applications.

Promising task is implementation of such networks in semiconductor technology, which makes it possible to place them in integrated circuit together with other analog and digital circuits with high density. Currently the most popular technology is complementary metal-oxide-semiconductor (CMOS), especially for processors and other logical devices fabrication. Therefore perspective basis to implement RC-networks is MOSFET-structure.

PROPOSAL AND Y-MATRIX OF R-C-NR NETWORK

Use of MOSFET as RC distributed element is known [1]. The basic idea is to use distributed gate capacitance and channel resistance of the MOSFET. In this case the device acts as simple RC circuit with distributed parameters, and channel resistance can be tuned by voltage connected to the gate. This principle is used for MOSFET-based implementation of low-pass filters [2], high-pass filters [3], and other frequency-selective circuits [4].

In this paper another idea is proposed – to use not only distributed channel resistance, but also gate distributed resistance, which is, of course, also presented in MOSFET because of non-zero polisilicon sheet resistance.

Proposed structure is depicted on Fig. 1a, which represents the depletion mode MOSFET consisting of polysilicon layer (gate), gate-oxide layer and the channel. Actually, the structure implements R-C-NR network with distributed parameters, where *r*, *c*, *Nr* are per unit length (PUL) parameters: gate resistance, gate-to-channel capacitance and channel resistance, respectively. Fig. 1b shows device symbol, where: terminal 5 represents "bulk" of the transistor and is intended for tune N – ratio between top and bottom resistances; 1, 2 – gate terminals; 3, 4 – drain and source terminals.

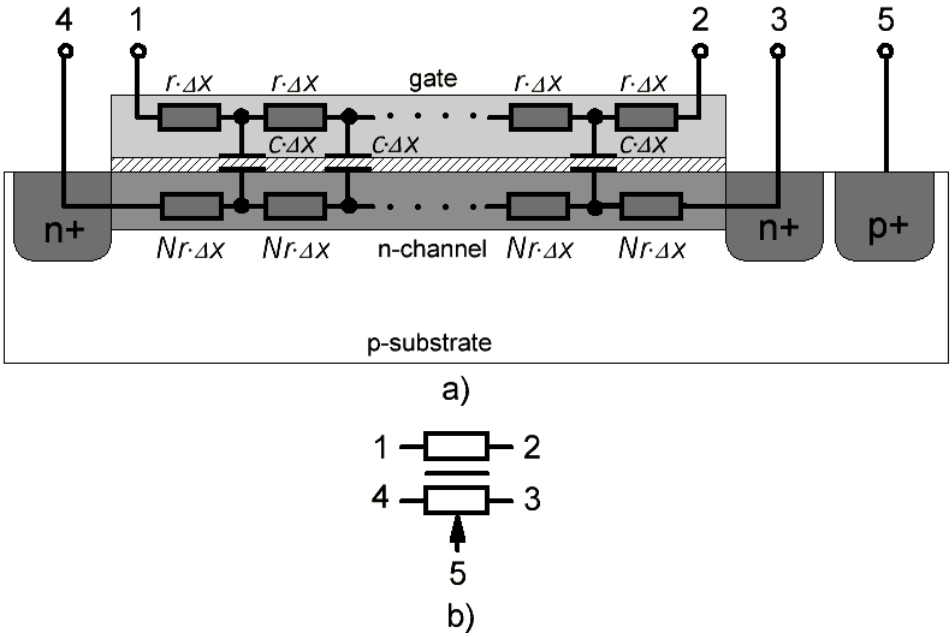

Figure 1. R-C-NR network with distributed parameters: cross section (a); symbol (b)

For modelling of the device conventional CAD could be used, but current MOSFET models don't represent distributed character of layers parameters, so they can't be used for this purpose. Thus, it is necessary to develop new model, which is able to be useable for modelling of the proposed structure.

Y-matrix (or nodal admittance matrix) of four-terminal system can be considered as the model. To derive the equations let's divide the structure into elementary sections of length Δx (Fig. 1a), and parameters are determined by used MOSFET. To derive parameters mentioned above classical MOSFET operation equations will be used [5, 6].

Top level resistance is determined by sheet resistance of the polysilicon R_s, channel length L and channel width W:

$$R = \frac{R_S \cdot L}{W}. \tag{1}$$

PUL resistance of the top layer in this case equals to:

$$r = \frac{R_S}{W}. \tag{2}$$

Some parameters depend on the operation mode of transistor, such as channel resistance and gate-to-channel capacitance. Transistor in triode region acts as a resistor controlled by

bias voltage, and the gate-to-channel capacitance as well as channel resistance are uniform over all channel length. So the linear mode is more preferable to R-C-NR network implementation. Following expressions will be derived with assumption that MOSFET operates in *linear mode*.

Next expression represents the PUL channel resistance of the MOSFET:

$$Nr = \frac{1}{\mu_n \cdot C_{ox} \cdot W \cdot \left(V_{gs} - V_{th}\right)}, \tag{3}$$

where μ_n – electrons mobility, C_{ox} – capacitance of the oxide layer, V_{gs} – gate-to-source voltage, V_{th} – threshold voltage.

To get N parameter let's divide (3) by (2):

$$N = \frac{1}{\mu_n \cdot C_{ox} \cdot R_s \cdot \left(V_{gs} - V_{th}\right)}. \tag{4}$$

Due to the body-effect the threshold voltage depends on substrate potential as following:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\varphi_F + V_{sb}|} - \sqrt{2|\varphi_F|}\right), \tag{5}$$

where V_{th0} – zero-biased threshold voltage (V_{sb} = 0), γ – body-effect coefficient, φ_F – electrostatic potential of the substrate (determined by technology), V_{sb} – source-to-bulk voltage. It means that channel resistance is affected by the voltage; therefore, R-C-NR network parameters can be changed by voltage connected to the substrate.

Gate-to-channel capacitance is determined by size, mode of operation and technology factors of the transistor. For linear mode transistor we can calculate the capacitance as:

$$C = WLC_{ox}. \tag{6}$$

To get PUL capacitance let's divide it by L:

$$c = WC_{ox}. \tag{7}$$

Thus, PUL conductivity of the oxide layer equals to:

$$y = j \cdot \omega \cdot c. \tag{8}$$

Now having all per unit length parameters of the layers, admittance matrix can be observed as [7]:

$$[Y] = \frac{1}{(1+N)R}\begin{vmatrix} \frac{\theta}{th\theta}+N & \frac{-\theta}{sh\theta}-N & \frac{\theta}{sh\theta}-1 & \frac{-\theta}{th\theta}+1 \\ \frac{-\theta}{sh\theta}-N & \frac{\theta}{th\theta}+N & \frac{-\theta}{th\theta}+1 & \frac{\theta}{sh\theta}-1 \\ \frac{\theta}{sh\theta}-1 & \frac{-\theta}{th\theta}+1 & \frac{\theta}{th\theta}+\frac{1}{N} & \frac{-\theta}{sh\theta}-\frac{1}{N} \\ \frac{-\theta}{th\theta}+1 & \frac{\theta}{sh\theta}-1 & \frac{-\theta}{sh\theta}-\frac{1}{N} & \frac{\theta}{th\theta}+\frac{1}{N} \end{vmatrix}, \tag{9}$$

where θ – propagation constant equals to:

$$\theta = \gamma \cdot L = \sqrt{(1+N)\cdot r \cdot y} \cdot L = \sqrt{j \cdot \omega \cdot \left(R_s \cdot C_{ox} + \frac{1}{\mu_n \cdot \left(V_{gs} - V_{th}\right)}\right)} \cdot L. \tag{10}$$

CONCLUSION

The model of semiconductor one-dimensional R-C-NR network based on MOSFET was developed, which makes it possible to research, simulate and design analog semiconductor circuits, particularly with fractional-order devices using. Model was derived using conventional MOSFET equations. Benefit of proposed structure is using of distributed gate resistance as additional element, which can be used for R-C-NR distributed network implementation. This network is tunable due to voltage dependency of channel-resistance, it means ratio between R and NR resistances can be changed by voltage. This feature is very useful for tunable analog filter realization.

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